

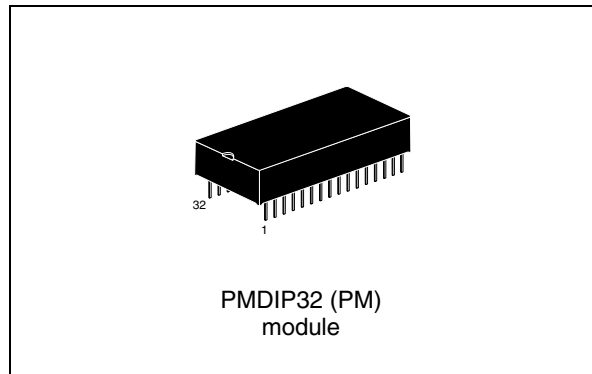


# M48Z512A M48Z512AY, M48Z512AV\*

4 Mbit (512 Kbit x 8) ZEROPOWER<sup>®</sup> SRAM

## Features

- Integrated, ultra low power SRAM, power-fail control circuit, and battery
- Conventional SRAM operation; unlimited WRITE cycles
- 10 years of data retention in the absence of power
- Automatic power-fail chip deselect and WRITE protection
- Two WRITE protect voltages:  
( $V_{PFD}$  = power-fail deselect voltage)
  - M48Z512A:  
 $V_{CC} = 4.75$  to  $5.5$  V,  $4.5$  V  $\leq V_{PFD} \leq 4.75$  V
  - M48Z512AY:  
 $V_{CC} = 4.5$  to  $5.5$  V,  $4.2$  V  $\leq V_{PFD} \leq 4.5$  V
  - M48Z512AV:  
 $V_{CC} = 3.0$  to  $3.6$  V,  $2.8$  V  $\leq V_{PFD} \leq 3.0$  V
- Battery internally isolated until power is applied
- Pin and function compatible with JEDEC standard 512 K x 8 SRAMs
- PMDIP32 is an ECOPACK<sup>®</sup> package



## Description

The M48Z512A/Y/V ZEROPOWER<sup>®</sup> RAM is a non-volatile, 4,194,304-bit static RAM organized as 524,288 words by 8 bits. The devices combine an internal lithium battery, a CMOS SRAM and a control circuit in a plastic, 32-pin DIP Module.

\*M48Z512AV Not for New Design  
(see M48Z512BV)

# Contents

<b>1</b>	<b>Device overview</b> .....	<b>5</b>
<b>2</b>	<b>Operating modes</b> .....	<b>7</b>
2.1	READ mode .....	7
2.2	WRITE mode .....	9
2.3	Data retention mode .....	11
2.4	V <sub>CC</sub> noise and negative going transients .....	12
<b>3</b>	<b>Maximum ratings</b> .....	<b>13</b>
<b>4</b>	<b>DC and AC parameters</b> .....	<b>14</b>
<b>5</b>	<b>Package mechanical data</b> .....	<b>17</b>
<b>6</b>	<b>Part numbering</b> .....	<b>18</b>
<b>7</b>	<b>Revision history</b> .....	<b>19</b>

## List of tables

Table 1.	Signal names . . . . .	5
Table 2.	Operating modes . . . . .	7
Table 3.	READ mode AC characteristics . . . . .	9
Table 4.	WRITE mode AC characteristics . . . . .	11
Table 5.	Absolute maximum ratings . . . . .	13
Table 6.	Operating and ac measurement conditions . . . . .	14
Table 7.	Capacitance . . . . .	14
Table 8.	DC characteristics . . . . .	15
Table 9.	Power down/up AC characteristics . . . . .	16
Table 10.	Power down/up trip points DC characteristics . . . . .	16
Table 11.	PMDIP32 – 32-pin plastic DIP module, package mechanical data. . . . .	17
Table 12.	Ordering information scheme . . . . .	18
Table 13.	Revision history . . . . .	19

## List of figures

Figure 1.	Logic diagram . . . . .	5
Figure 2.	DIP connections . . . . .	6
Figure 3.	Block diagram . . . . .	6
Figure 4.	Chip enable or output enable controlled, READ mode AC waveforms. . . . .	8
Figure 5.	Address controlled, READ mode AC waveforms . . . . .	8
Figure 6.	WRITE enable controlled, WRITE AC waveforms . . . . .	10
Figure 7.	Chip enable controlled, WRITE AC waveforms . . . . .	10
Figure 8.	Supply voltage protection . . . . .	12
Figure 9.	AC measurement load circuit . . . . .	14
Figure 10.	Power down/up mode AC waveforms. . . . .	15
Figure 11.	PMDIP32 – 32-pin plastic DIP module, package outline . . . . .	17

# 1 Device overview

Figure 1. Logic diagram

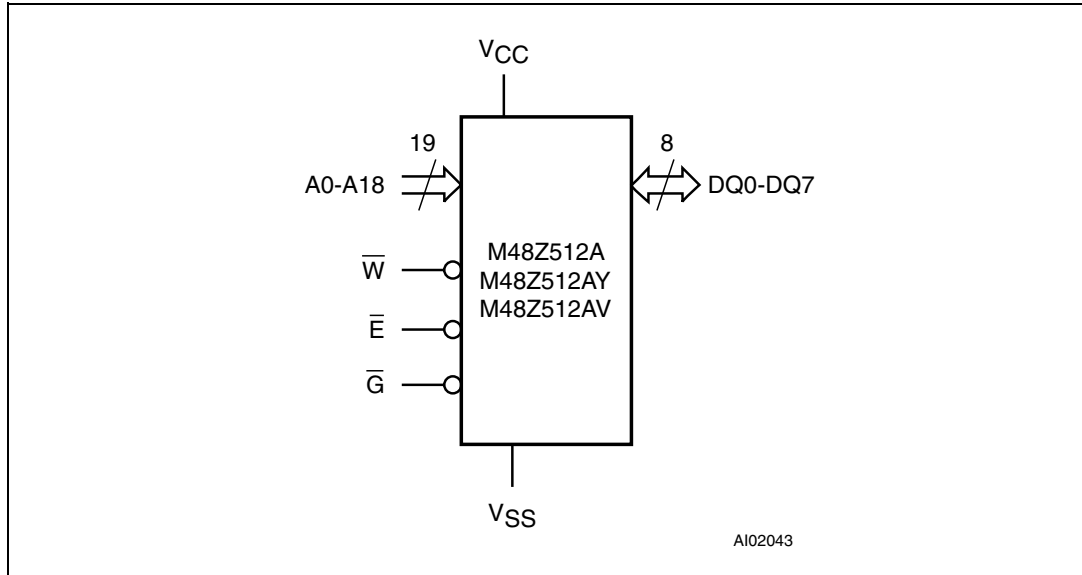


Table 1. Signal names

A0-A18	Address inputs
DQ0-DQ7	Data inputs/outputs
$\bar{E}$	Chip enable input
$\bar{G}$	Output enable input
$\bar{W}$	WRITE enable input
$V_{CC}$	Supply voltage
$V_{SS}$	Ground

Figure 2. DIP connections

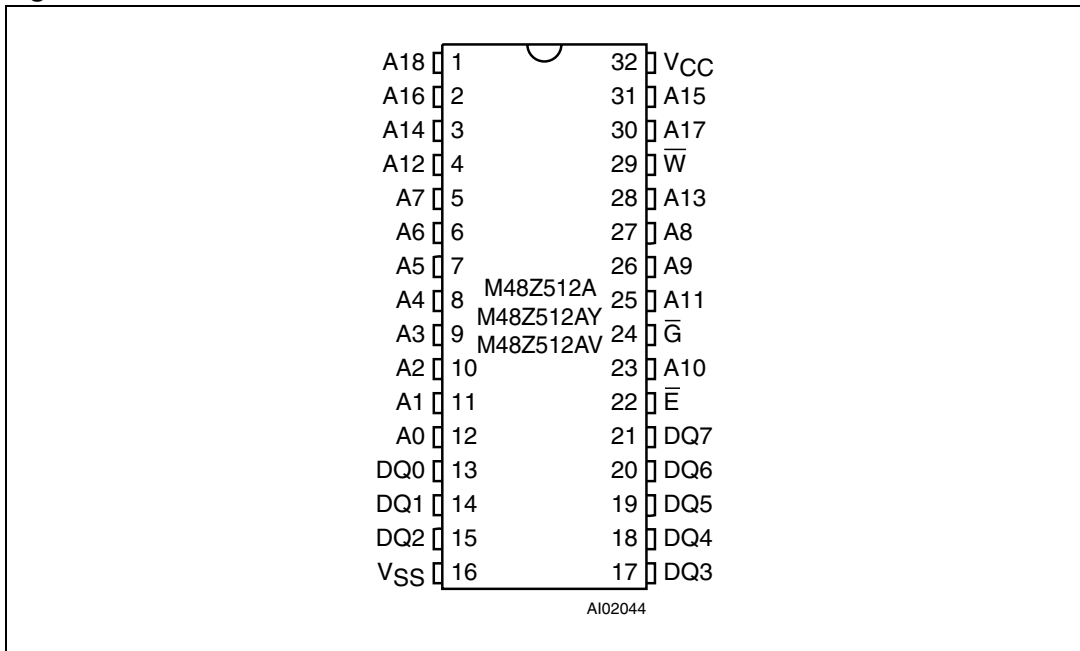
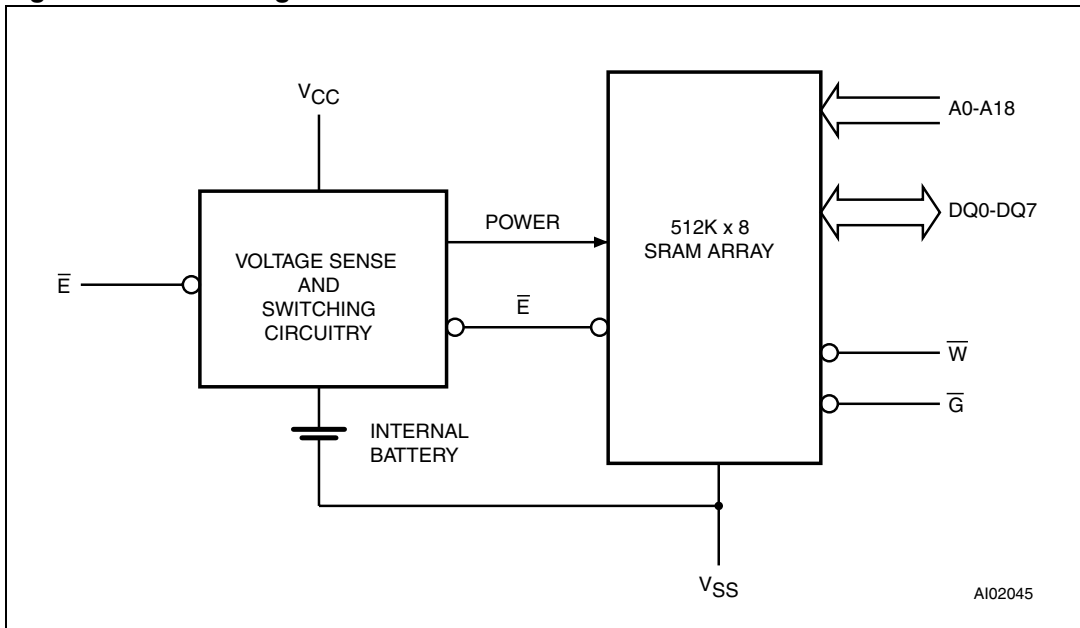


Figure 3. Block diagram



## 2 Operating modes

The M48Z512A/Y/V also has its own power-fail detect circuit. The control circuitry constantly monitors the single  $V_{CC}$  supply for an out of tolerance condition. When  $V_{CC}$  is out of tolerance, the circuit WRITE protects the SRAM, providing a high degree of data security in the midst of unpredictable system operation brought on by low  $V_{CC}$ . As  $V_{CC}$  falls below the switchover voltage ( $V_{SO}$ ), the control circuitry connects the battery which maintains data until valid power returns.

The ZEROPOWER<sup>®</sup> RAM replaces industry standard SRAMs. It provides the nonvolatility of PROMs without any requirement for special WRITE timing or limitations on the number of WRITES that can be performed.

**Table 2. Operating modes<sup>(1)</sup>**

Mode	$V_{CC}$	$\bar{E}$	$\bar{G}$	$\bar{W}$	DQ0-DQ7	Power
Deselect	4.75 to 5.5 V or 4.5 to 5.5 V or 3.0 to 3.6 V	$V_{IH}$	X	X	High Z	Standby
WRITE		$V_{IL}$	X	$V_{IL}$	$D_{IN}$	Active
READ		$V_{IL}$	$V_{IL}$	$V_{IH}$	$D_{OUT}$	Active
READ		$V_{IL}$	$V_{IH}$	$V_{IH}$	High Z	Active
Deselect	$V_{SO}$ to $V_{PFD}$ (min) <sup>(2)</sup>	X	X	X	High Z	CMOS standby
Deselect	$\leq V_{SO}$ <sup>(2)</sup>	X	X	X	High Z	Battery backup mode

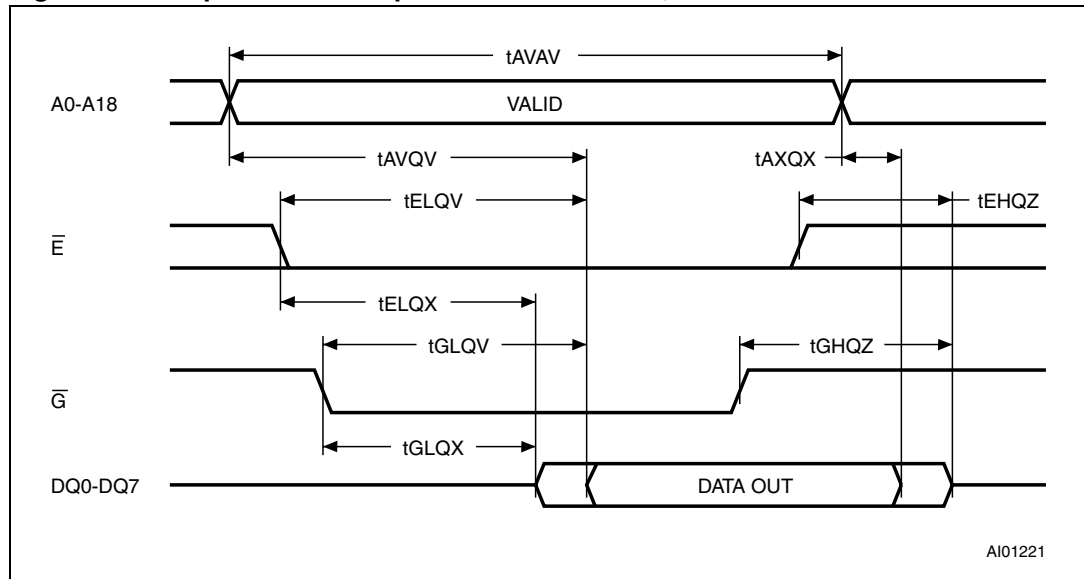
1. See [Table 10 on page 16](#) for details.

2. X =  $V_{IH}$  or  $V_{IL}$ ;  $V_{SO}$  = battery backup switchover voltage.

### 2.1 READ mode

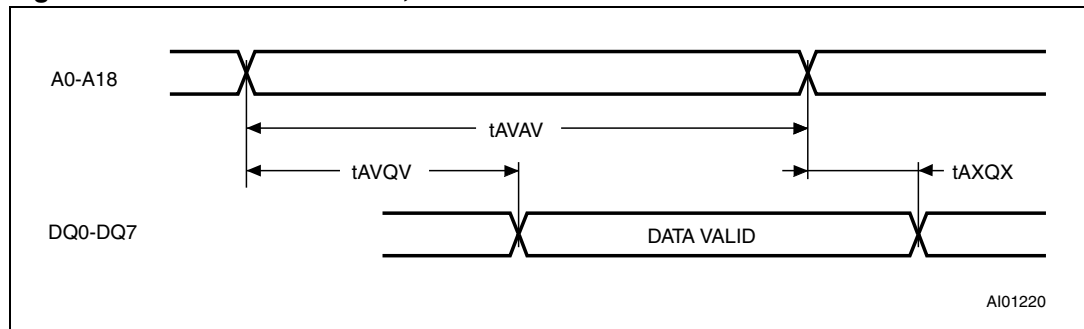
The M48Z512A/Y/V is in the READ mode whenever  $\bar{W}$  (WRITE Enable) is high and  $\bar{E}$  (chip enable) is low. The device architecture allows ripple-through access of data from eight of 4,194,304 locations in the static storage array. Thus, the unique address specified by the 19 address inputs defines which one of the 524,288 bytes of data is to be accessed. Valid data will be available at the data I/O pins within address access time ( $t_{AVQV}$ ) after the last address input signal is stable, providing that the  $\bar{E}$  (chip enable) and  $\bar{G}$  (output enable) access times are also satisfied. If the  $\bar{E}$  and  $\bar{G}$  access times are not met, valid data will be available after the later of chip enable access time ( $t_{ELQV}$ ) or output enable access Time ( $t_{GLQV}$ ). The state of the eight three-state data I/O signals is controlled by  $\bar{E}$  and  $\bar{G}$ . If the outputs are activated before  $t_{AVQV}$ , the data lines will be driven to an indeterminate state until  $t_{AVQV}$ . If the address inputs are changed while  $\bar{E}$  and  $\bar{G}$  remain low, output data will remain valid for output data hold time ( $t_{AXQX}$ ) but will go indeterminate until the next address access.

**Figure 4. Chip enable or output enable controlled, READ mode AC waveforms**



1. WRITE Enable ( $\bar{W}$ ) = high

**Figure 5. Address controlled, READ mode AC waveforms**



1. Chip enable ( $\bar{E}$ ) and output enable ( $\bar{G}$ ) = low, WRITE enable ( $\bar{W}$ ) = high



**Table 3. READ mode AC characteristics**

Symbol	Parameter <sup>(1)</sup>	M48Z512A/Y -70		M48Z512A/Y/V -85		Unit
		Min	Max	Min	Max	
t <sub>AVAV</sub>	READ cycle time	70		85		ns
t <sub>AVQV</sub>	Address valid to output valid		70		85	ns
t <sub>ELQV</sub>	Chip enable low to output valid		70		85	ns
t <sub>GLQV</sub>	Output enable low to output valid		35		45	ns
t <sub>ELQX</sub> <sup>(2)</sup>	Chip enable low to output transition	5		5		ns
t <sub>GLQX</sub> <sup>(2)</sup>	Output enable low to output transition	5		5		ns
t <sub>EHQZ</sub> <sup>(2)</sup>	Chip enable high to output Hi-Z		30		35	ns
t <sub>GHQZ</sub> <sup>(2)</sup>	Output enable high to output Hi-Z		20		25	ns
t <sub>AXQX</sub>	Address transition to output transition	5		5		ns

1. Valid for ambient operating temperature: T<sub>A</sub> = 0 to 70°C or -40 to 85°C; V<sub>CC</sub> = 4.75 to 5.5 V, 4.5 to 5.5 V, or 3.0 to 3.6 V (except where noted).

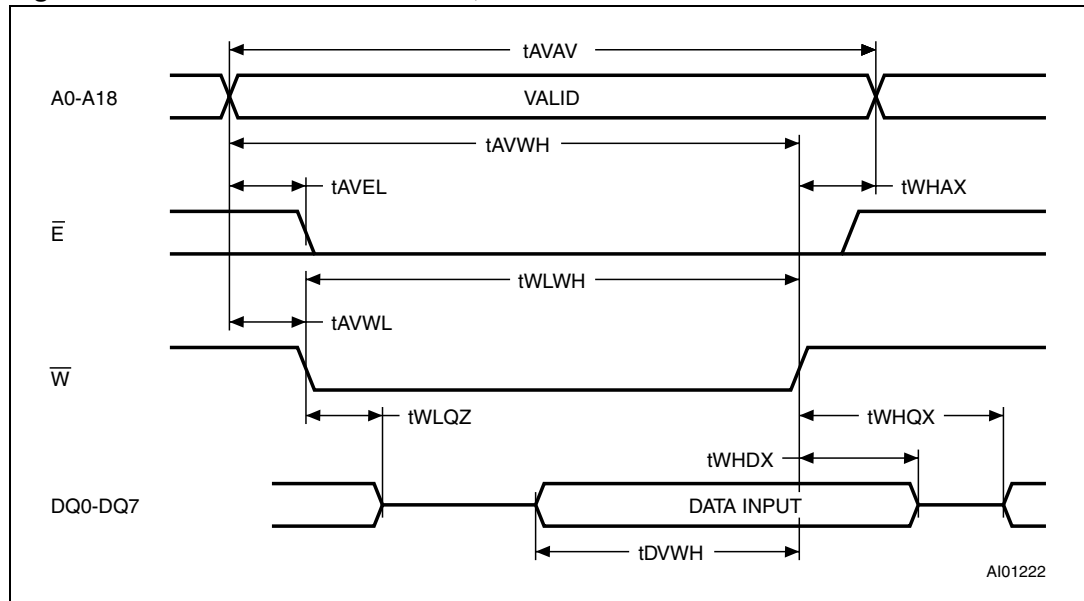
2. C<sub>L</sub> = 5 pF.

## 2.2 WRITE mode

The M48Z512A/Y/V is in the WRITE mode whenever  $\overline{W}$  and  $\overline{E}$  are active. The start of a WRITE is referenced from the latter occurring falling edge of  $\overline{W}$  or  $\overline{E}$ . A WRITE is terminated by the earlier rising edge of  $\overline{W}$  or  $\overline{E}$ .

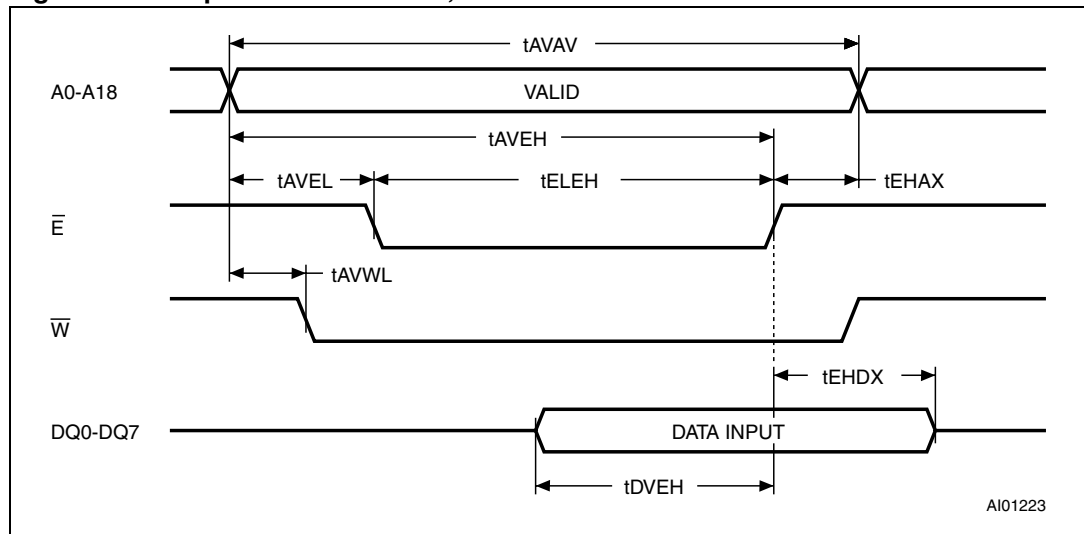
The addresses must be held valid throughout the cycle.  $\overline{E}$  or  $\overline{W}$  must return high for a minimum of t<sub>EHAX</sub> from  $\overline{E}$  or t<sub>WHAX</sub> from  $\overline{W}$  prior to the initiation of another READ or WRITE cycle. Data-in must be valid t<sub>DVEH</sub> or t<sub>DVWH</sub> prior to the end of WRITE and remain valid for t<sub>EHDX</sub> or t<sub>WHDX</sub> afterward.  $\overline{G}$  should be kept high during WRITE cycles to avoid bus contention; although, if the output bus has been activated by a low on  $\overline{E}$  and  $\overline{G}$ , a low on  $\overline{W}$  will disable the outputs t<sub>WLQZ</sub> after  $\overline{W}$  falls.

**Figure 6. WRITE enable controlled, WRITE AC waveforms**



1. Output enable ( $\bar{G}$ ) = high.

**Figure 7. Chip enable controlled, WRITE AC waveforms**



1. Output enable ( $\bar{G}$ ) = high.

Table 4. WRITE mode AC characteristics

Symbol	Parameter <sup>(1)</sup>	M48Z512A/Y -70		M48Z512A/Y/V -85		Unit
		Min	Max	Min	Max	
t <sub>AVAV</sub>	WRITE cycle time	70		85		ns
t <sub>AVWL</sub>	Address valid to WRITE enable low	0		0		ns
t <sub>AVEL</sub>	Address valid to chip enable low	0		0		ns
t <sub>WLWH</sub>	WRITE enable pulse width	55		65		ns
t <sub>ELEH</sub>	Chip enable low to chip enable high	55		75		ns
t <sub>WHAX</sub>	WRITE enable high to address transition	5		5		ns
t <sub>EHAX</sub>	Chip enable high to address transition	15		15		ns
t <sub>DVWH</sub>	Input valid to WRITE enable high	30		35		ns
t <sub>DVEH</sub>	Input valid to chip enable high	30		35		ns
t <sub>WHDX</sub>	WRITE enable high to input transition	0		0		ns
t <sub>EHDX</sub>	Chip enable high to input transition	10		10		ns
t <sub>WLQZ</sub> <sup>(2)(3)</sup>	WRITE enable low to output Hi-Z		25		30	ns
t <sub>AVWH</sub>	Address valid to WRITE enable high	65		75		ns
t <sub>AVEH</sub>	Address valid to chip enable high	65		75		ns
t <sub>WHQX</sub> <sup>(2)(3)</sup>	WRITE enable high to output transition	5		5		ns

1. Valid for ambient operating temperature: T<sub>A</sub> = 0 to 70°C or -40 to 85°C; V<sub>CC</sub> = 4.75 to 5.5 V, 4.5 to 5.5 V or 3.0 to 3.6 V (except where noted).

2. C<sub>L</sub> = 5 pF.

3. If  $\overline{E}$  goes low simultaneously with  $\overline{W}$  going low, the outputs remain in the high impedance state.

## 2.3 Data retention mode

With valid V<sub>CC</sub> applied, the M48Z512A/Y/V operates as a conventional BYTEWIDE™ static RAM. Should the supply voltage decay, the RAM will automatically power-fail deselect, WRITE protecting itself t<sub>WP</sub> after V<sub>CC</sub> falls below V<sub>PFD</sub>. All outputs become high impedance, and all inputs are treated as “don't care.”

If power fail detection occurs during a valid access, the memory cycle continues to completion. If the memory cycle fails to terminate within the time t<sub>WP</sub>, WRITE protection takes place. When V<sub>CC</sub> drops below V<sub>SO</sub>, the control circuit switches power to the internal energy source which preserves data.

The internal coin cell will maintain data in the M48Z512A/Y/V after the initial application of V<sub>CC</sub> for an accumulated period of at least 10 years when V<sub>CC</sub> is less than V<sub>SO</sub>. As system power returns and V<sub>CC</sub> rises above V<sub>SO</sub>, the battery is disconnected, and the power supply is switched to external V<sub>CC</sub>. WRITE protection continues for t<sub>ER</sub> after V<sub>CC</sub> reaches V<sub>PFD</sub> to allow for processor stabilization. After t<sub>ER</sub>, normal RAM operation can resume.

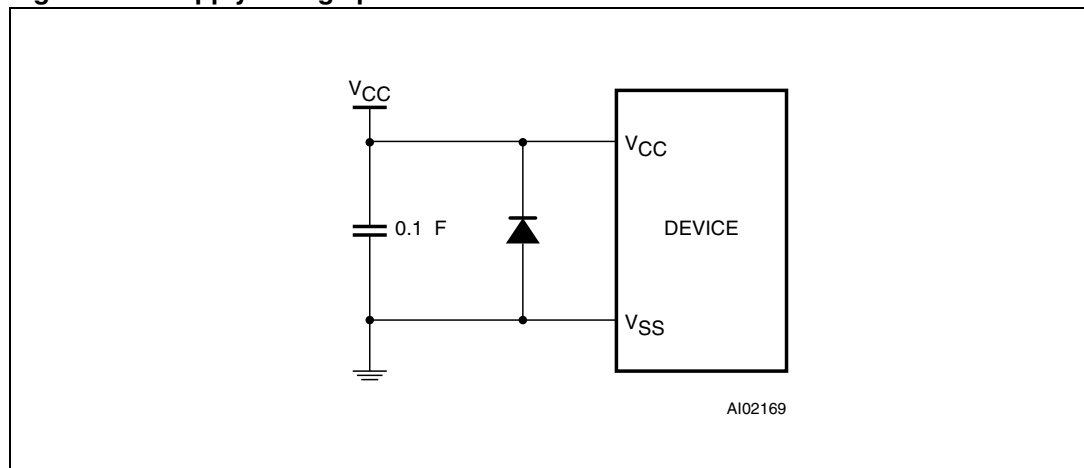
For more information on battery storage life refer to the application note AN1012.

## 2.4 V<sub>CC</sub> noise and negative going transients

I<sub>CC</sub> transients, including those produced by output switching, can produce voltage fluctuations, resulting in spikes on the V<sub>CC</sub> bus. These transients can be reduced if capacitors are used to store energy which stabilizes the V<sub>CC</sub> bus. The energy stored in the bypass capacitors will be released as low going spikes are generated or energy will be absorbed when overshoots occur. A ceramic bypass capacitor value of 0.1 μF (see [Figure 8](#)) is recommended in order to provide the needed filtering.

In addition to transients that are caused by normal SRAM operation, power cycling can generate negative voltage spikes on V<sub>CC</sub> that drive it to values below V<sub>SS</sub> by as much as one volt. These negative spikes can cause data corruption in the SRAM while in battery backup mode. To protect from these voltage spikes, ST recommends connecting a schottky diode from V<sub>CC</sub> to V<sub>SS</sub> (cathode connected to V<sub>CC</sub>, anode to V<sub>SS</sub>). (Schottky diode 1N5817 is recommended for through hole and MBR5120T3 is recommended for surface-mount).

**Figure 8. Supply voltage protection**



### 3 Maximum ratings

Stressing the device above the rating listed in the absolute maximum ratings table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.

**Table 5. Absolute maximum ratings**

Symbol	Parameter		Value	Unit
T <sub>A</sub>	Ambient operating temperature	Grade 1	0 to 70	°C
		Grade 6	-40 to 85	
T <sub>STG</sub>	Storage temperature (V <sub>CC</sub> off)		-40 to 85	°C
T <sub>BIAS</sub>	Temperature under bias	Grade 1	0 to 70	°C
		Grade 6	-40 to 85	
T <sub>SLD</sub> <sup>(1)</sup>	Lead solder temperature for 10 seconds		260	°C
V <sub>IO</sub>	Input or output voltages		-0.3 to 7	V
V <sub>CC</sub>	Supply voltage	M48Z512A/512AY	-0.3 to 7.0	V
		M48Z512AV	-0.3 to 4.6	V
I <sub>O</sub>	Output current		20	mA
P <sub>D</sub>	Power dissipation		1	W

1. For DIP package: soldering temperature not to exceed 260°C for 10 seconds (total thermal budget not to exceed 150°C for longer than 30 seconds). No preheating above 150°C, or direct exposure to IR reflow (or IR preheat) allowed, to avoid damaging the lithium battery.

**Caution:** *Negative undershoots below -0.3 V are not allowed on any pin while in the battery backup mode.*

## 4 DC and AC parameters

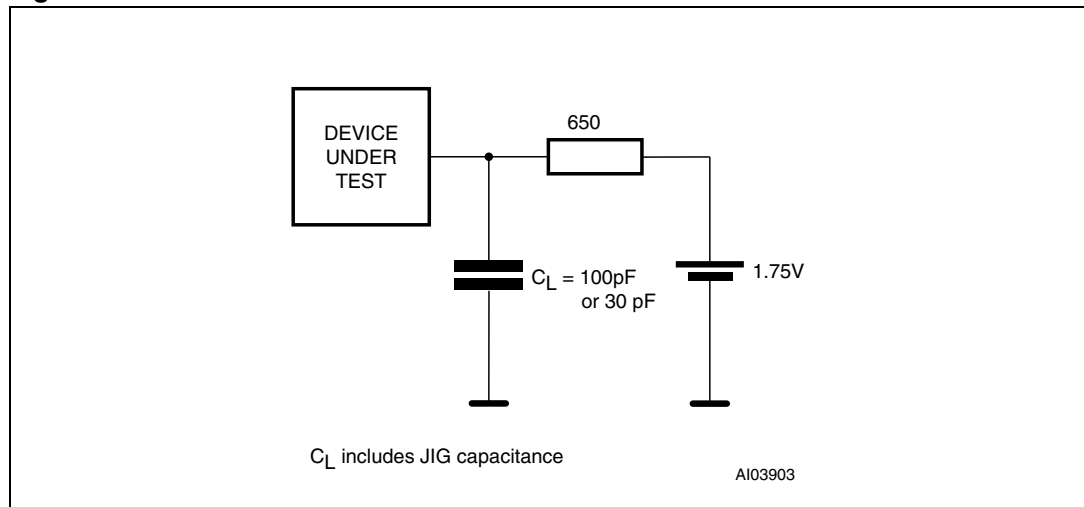
This section summarizes the operating and measurement conditions, as well as the dc and ac characteristics of the device. The parameters in the following DC and AC characteristic tables are derived from tests performed under the measurement conditions listed in the relevant tables. Designers should check that the operating conditions in their projects match the measurement conditions when using the quoted parameters.

**Table 6. Operating and ac measurement conditions<sup>(1)</sup>**

Parameter		M48Z512A/512AY	M48Z512AV	Unit
Supply voltage ( $V_{CC}$ )		4.75 to 5.5 V or 4.5 to 5.5	3.0 to 3.6	V
Ambient operating temperature ( $T_A$ )	Grade 1	0 to 70	0 to 70	°C
	Grade 6	-40 to 85	-40 to 85	
Load capacitance ( $C_L$ )		100	50	pF
Input rise and fall times		≤ 5	≤ 5	ns
Input pulse voltages		0 to 3	0 to 3	V
Input and output timing ref. voltages		1.5	1.5	V

1. Output Hi-Z is defined as the point where data is no longer driven.

**Figure 9. AC measurement load circuit**



1. Excluding open drain output pins; 50 pF for M48Z512AV.

**Table 7. Capacitance**

Symbol	Parameter <sup>(1)(2)</sup>	Min	Max	Unit
$C_{IN}$	Input capacitance		10	pF
$C_{IO}^{(3)}$	Input/output capacitance		10	pF

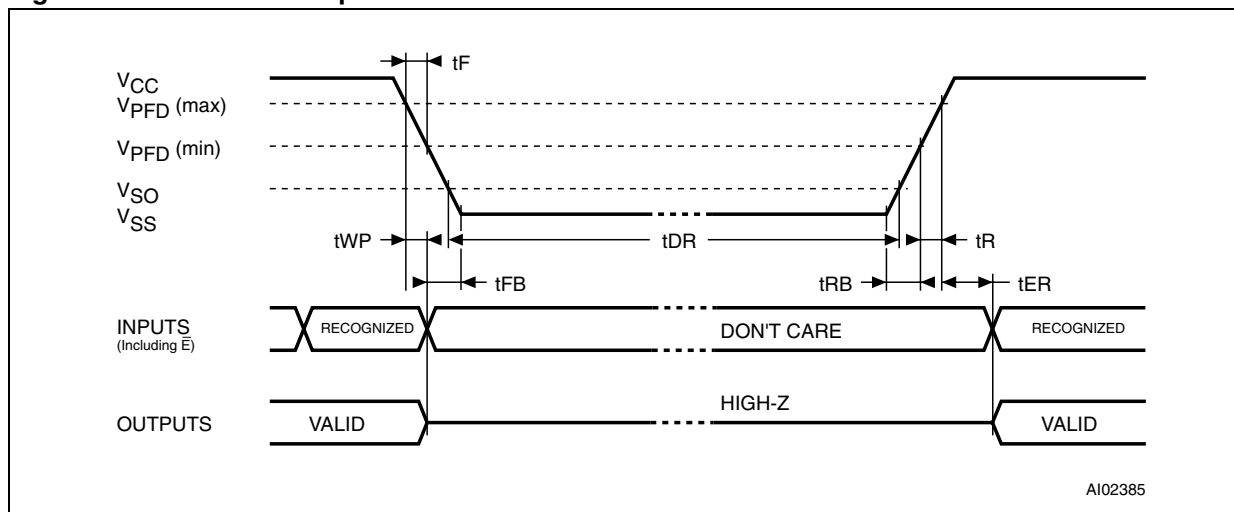
1. Effective capacitance measured with power supply at 5 V (M48Z512A/Y) or 3.3 V (M48Z512AV); sampled only, not 100% tested.
2. Outputs deselected.
3. At 25°C.

**Table 8. DC characteristics**

Sym	Parameter	Test condition <sup>(1)</sup>	M48Z512A/Y -70		M48Z512AV -85		Unit
			Min	Max	Min	Max	
$I_{LI}^{(2)}$	Input leakage current	$0V \leq V_{IN} \leq V_{CC}$		$\pm 1$		$\pm 1$	$\mu A$
$I_{LO}^{(2)}$	Output leakage current	$0V \leq V_{OUT} \leq V_{CC}$		$\pm 1$		$\pm 1$	$\mu A$
$I_{CC}$	Supply current	$\bar{E} = V_{IL}$ outputs open		115		50	mA
$I_{CC1}$	Supply current (standby) TTL	$\bar{E} = V_{IH}$		10		4	mA
$I_{CC2}$	Supply current (standby) CMOS	$\bar{E} \geq V_{CC} - 0.2V$		5		3	mA
$V_{IL}$	Input low voltage		-0.3	0.8	-0.3	0.6	V
$V_{IH}$	Input high voltage		2.2	$V_{CC} + 0.3$	2.2	$V_{CC} + 0.3$	V
$V_{OL}$	Output low voltage	$I_{OL} = 2.1mA$		0.4		0.4	V
$V_{OH}$	Output high voltage	$I_{OH} = -1mA$	2.4		2.2		V

- Valid for ambient operating temperature:  $T_A = 0$  to  $70^\circ C$  or  $-40$  to  $85^\circ C$ ;  $V_{CC} = 4.75$  to  $5.5$  V,  $4.5$  to  $5.5$  V, or  $3.0$  to  $3.6$  V (except where noted).
- Outputs deselected.

**Figure 10. Power down/up mode AC waveforms**



**Table 9. Power down/up AC characteristics**

Symbol	Parameter <sup>(1)</sup>	Min	Max	Unit	
$t_F^{(2)}$	$V_{PFD} (max)$ to $V_{PFD} (min)$ $V_{CC}$ fall time	300		$\mu s$	
$t_{FB}^{(3)}$	$V_{PFD} (min)$ to $V_{SS}$ $V_{CC}$ fall time	M48Z512A/Y	10	$\mu s$	
		M48Z512AV	150		
$t_R$	$V_{PFD} (min)$ to $V_{PFD} (max)$ $V_{CC}$ rise time	10		$\mu s$	
$t_{RB}$	$V_{SS}$ to $V_{PFD} (min)$ $V_{CC}$ rise time	1		$\mu s$	
$t_{WPT}$	WRITE protect time	M48Z512A/Y	40	150	$\mu s$
		M48Z512AV	40	250	
$t_{ER}$	$\bar{E}$ recovery time	40	120	ms	

- Valid for ambient operating temperature:  $T_A = 0$  to  $70^\circ C$  or  $-40$  to  $85^\circ C$ ;  $V_{CC} = 4.75$  to  $5.5$  V,  $4.5$  to  $5.5$  V, or  $3.0$  to  $3.6$  V (except where noted).
- $V_{PFD} (max)$  to  $V_{PFD} (min)$  fall time of less than  $t_F$  may result in deselection/WRITE protection not occurring until  $200 \mu s$  after  $V_{CC}$  passes  $V_{PFD} (min)$ .
- $V_{PFD} (min)$  to  $V_{SS}$  fall time of less than  $t_{FB}$  may cause corruption of RAM data.

**Table 10. Power down/up trip points DC characteristics**

Symbol	Parameter <sup>(1)(2)</sup>	Min	Typ	Max	Unit	
$V_{PFD}$	Power-fail deselect voltage	M48Z512A	4.5	4.6	4.75	V
		M48Z512AY	4.2	4.3	4.5	V
		M48Z512AV	2.8	2.9	3.0	V
$V_{SO}$	Battery backup switchover voltage	M48Z512A/Y		3.0		V
		M48Z512AV		2.5		V
$t_{DR}^{(3)}$	Expected data retention time	10			Years	

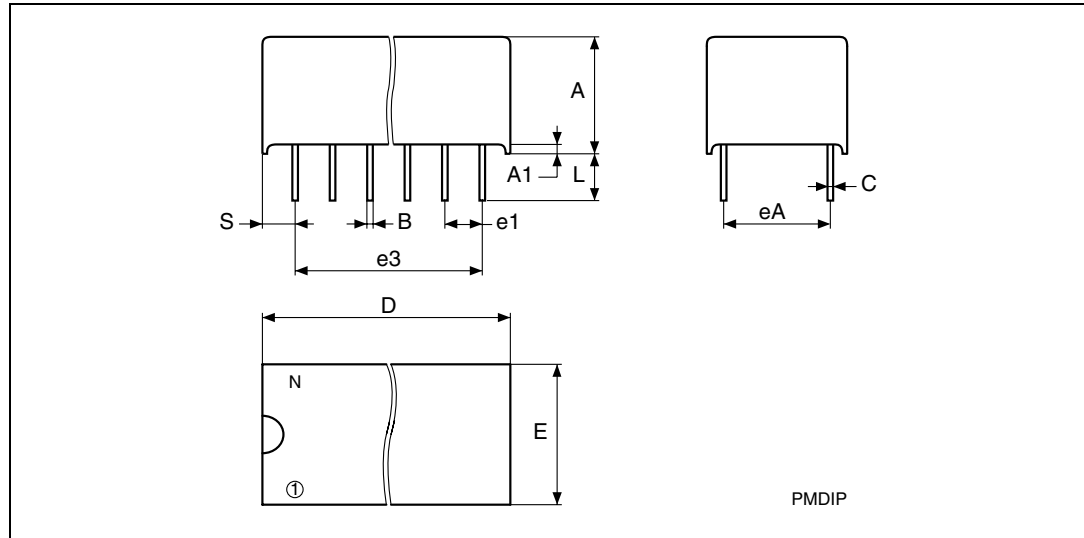
- All voltages referenced to  $V_{SS}$ .
- Valid for ambient operating temperature:  $T_A = 0$  to  $70^\circ C$  or  $-40$  to  $85^\circ C$ ;  $V_{CC} = 4.75$  to  $5.5$  V,  $4.5$  to  $5.5$  V, or  $3.0$  to  $3.6$  V (except where noted).
- At  $25^\circ C$ ;  $V_{CC} = 0$  V.



## 5 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK<sup>®</sup> packages. These packages have a lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK is an ST trademark. ECOPACK specifications are available at: [www.st.com](http://www.st.com).

**Figure 11. PMDIP32 – 32-pin plastic DIP module, package outline**



1. Drawing is not to scale.

**Table 11. PMDIP32 – 32-pin plastic DIP module, package mechanical data**

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		9.27	9.52		0.365	0.375
A1		0.38			0.015	
B		0.43	0.59		0.017	0.023
C		0.20	0.33		0.008	0.013
D		42.42	43.18		1.670	1.700
E		18.03	18.80		0.710	0.740
e1		2.29	2.79		0.090	0.110
e3	38.10			1.50		
eA		14.99	16.00		0.590	0.630
L		3.05	3.81		0.120	0.150
S		1.91	2.79		0.075	0.110
N		32			32	

## 6 Part numbering

**Table 12. Ordering information scheme**

Example:	M48Z	512AY	-70	PM	1
<b>Device type</b>	M48Z				
<b>Supply voltage and WRITE Protect voltage</b>		512A = $V_{CC} = 4.75$ to $5.5V$ ; $V_{PFD} = 4.5$ to $4.75V$ 512AY = $V_{CC} = 4.5$ to $5.5V$ ; $V_{PFD} = 4.2$ to $4.5V$ 512AV <sup>(1)</sup> = $V_{CC} = 3.0$ to $3.6V$ ; $V_{PFD} = 2.8$ to $3.0V$			
<b>Speed</b>			-70 = 70ns (for M48Z512A/Y) -85 = 85ns (for M48Z512A/Y/V)		
<b>Package</b>				PM = PMDIP32	
<b>Temperature range</b>					1 = 0 to 70°C 6 = -40 to 85°C

1. M48Z512AV Not for New Design (see M48Z512BV)

For other options, or for more information on any aspect of this device, please contact the ST sales office nearest you.

## 7 Revision history

**Table 13. Revision history**

Date	Revision	Changes
March 2000	1	First issue
19-Jul-00	1.1	M48Z12AV added
15-Jan-01	1.2	Changed LPSRAM device ( <a href="#">Table 2</a> )
19-Dec-01	2	Reformatted; added temperature information ( <a href="#">Table 3</a> , <a href="#">Table 4</a> , <a href="#">Table 7</a> , <a href="#">Table 8</a> , <a href="#">Table 9</a> , and <a href="#">Table 10</a> ); remove chipset option from Ordering Information ( <a href="#">Table 12</a> ); remove reference to “clock”
08-Feb-02	2.1	Remove 85ns speed grade ( <a href="#">Table 3</a> , <a href="#">Table 4</a> , and <a href="#">Table 8</a> )
29-May-02	2.2	Modify reflow time and temperature footnotes ( <a href="#">Table 5</a> )
18-Nov-02	2.3	Modified SMT text ( <a href="#">Figure 1</a> , <a href="#">Figure</a> , and <a href="#">Table 2</a> )
17-Sep-03	2.4	Remove references to M68xxx (obsolete) part ( <a href="#">Figure</a> and <a href="#">Table 2</a> ); update disclaimer
30-Nov-04	3	Reformatted; remove extended temperature references ( <a href="#">Table 12</a> )
21-Dec-04	4	Update Marketing Status for qualification, correct drawing ( <a href="#">Figure</a> and <a href="#">Table 12</a> )
22-Feb-05	5	IR reflow, SO package updates ( <a href="#">Table 5</a> )
21-Dec-2006	6	Document reformatted. ECOPACK package text added on coverpage. Note 2 concerning Leaded SOIC package removed below <a href="#">Table 5</a> . Updated PMDIP32 package mechanical data in <a href="#">Section 5: Package mechanical data</a> ; updated T <sub>A</sub> to include Grade 1 (0 to 70°C) and Grade 6 (-40 to 85°C).
7-Nov-2008	7	Indicated that M48Z512AV is Not for New Design; removed all SNAPHAT <sup>®</sup> battery and SOIC package references; updated <a href="#">Section 5: Package mechanical data</a> .

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